**Practical No.1**

Aim: Logic Gates Truth Table Verificat Not Gate (Inverter): Invents the input

1. AND Gate : Output is true only if all inputs are true
2. OR Gate: Output is true if at least one input is true
3. NAND Gate : Inverse of AND
4. NOR Gate : Inverse of OR
5. XOR Gate (Exclusive OR): Output is true if inputs are different
6. XNOR Gate: Output is true if inputs are the same

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**Practical No.2**

AIM: Boolean Expression Simplification

1. Definition And Simplification
2. Realize in Logisim
3. K-map / SOP Confirmation

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**Practical No.3**

Aim: Design and verify a half/full adder

1. Half Adder
2. Full Adder

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**Practical No.4**

AIM:Design and verify half/fullsubtractor

1. Subtractor
2. Half Subtractor
3. Full Subtractor

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**Practical No.5**

AIM:Design a 4 bit magnitude comparator using combinational circuit

1. MAGNITUDE COMPARATOR IN DIGITAL LOGIC
2. 4 BIT MAGNITUDE COMPARATOR
3. 1 BIT MAGNITUDE COMPARATOR

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**Practical No.6**

AIM: Flip – Flop Implementation

1. SR Flip – Flop
2. D Flip- Flop
3. Jk Flip-Flop

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**Practical No.7**

AIM: Design Counter Operation Verification

1. 4-Bit Magnitude Comparator in Logisim
2. T flip-flop
3. 4 BIT SYNCHRONOUS (UP) COUNTER
4. 4 BIT ASYNCHRONOUS (DOWN) COUNTER:

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**Practical No.8**

AIM: Design the Shift Register

* 1. What is 4-Bit Shift Register
  2. Uses of 4-Bit Shift Register
  3. Shift Register

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**Practical No.9**

AIM:Design and implement a 3-bit binary ripple counter

Using Multiplexers/Demultiplexers

1. Multiplexers
2. Demultiplexers

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